

PiezoMUMPsTM Design Handbook

a MUMPs® process

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Chapter 1

Piezoelectric Micromachining Process

1.1 Introduction

The Multi-User MEMS Processes, or MUMPs[®], is a commercial program that provides cost-effective, proof-of-concept MEMS fabrication to industry, universities, and government worldwide. MEMSCAP offers three standard processes as part of the MUMPs[®] program: **PolyMUMPs**, a three-layer polysilicon surface micromachining process; **MetalMUMPs**, an electroplated nickel process; and **SOIMUMPs**, a silicon-on-insulator micromachining process. A fourth process, **PiezoMUMPs**, is being introduced with this document.

The following is a general process description and user guide for PiezoMUMPs, which is designed for general-purpose micromachining of piezoelectric devices in a Silicon-on-Insulator framework. Chapter 1 of this document explains the process step-by-step, while Chapter 2 outlines the design rules for the process.

Though this document is geared toward designers who do not have a strong background in microfabrication, it contains information that is useful to all MUMPs[®] users. Regardless of the level of the designer, we strongly recommend all users of PiezoMUMPs review this document prior to submitting a design.

The process is designed to be as general as possible, and to be capable of supporting many different designs on a single silicon wafer. Since the process was not optimized with the purpose of fabricating any one specific device, the thickness of the layers were chosen to suit most users, and the design rules were chosen conservatively to guarantee the highest yield possible.

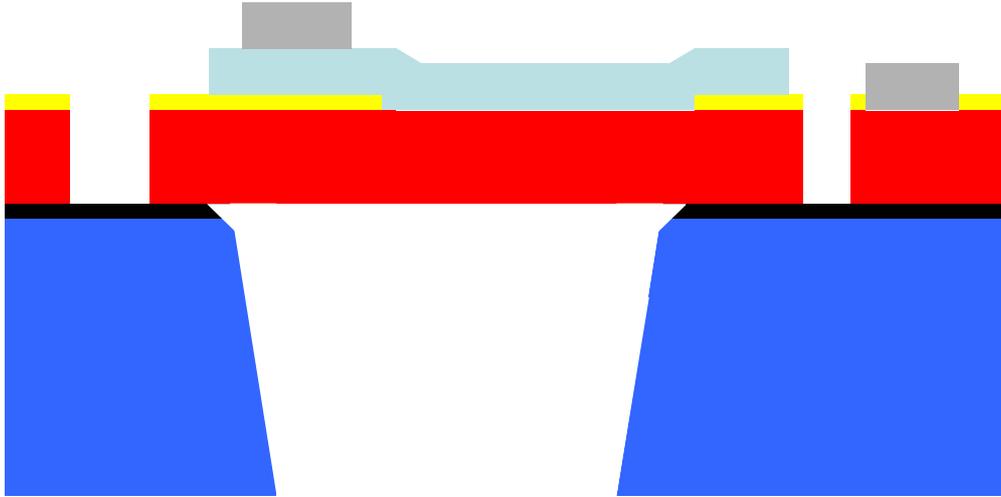


FIGURE 1.1. Cross sectional view showing all layers of the PiezoMUMPs process (not to scale).

Figure 1.1 is a cross section of the silicon-on-insulator micromachining PiezoMUMPs process. This process has the following general features:

1. A silicon-on-insulator (SOI) wafer is used as the starting substrate. The substrate has the following characteristics:
 - 150 mm (100) oriented SOI wafer
 - Silicon thickness: $10 \pm 1 \mu\text{m}$
 - Oxide thickness: $1 \pm 0.05 \mu\text{m}$
 - Handle wafer (Substrate) thickness: $400 \pm 5 \mu\text{m}$
2. The Silicon layer is doped, then patterned and etched down to the Oxide layer. This layer can be used for mechanical structures, resistor structures, and/or electrical routing.
3. The Substrate can be patterned and etched from the “bottom” side to the Oxide layer. This allows for through-hole structures.
4. A thermal oxide layer is patterned and etched to provide isolation between the SOI layer and the AlN and PadMetal layers.
5. A piezoelectric layer, AlN, allows for the development of piezoelectric sensors.
6. A pad-metal feature that allows finer metal features and precision alignment but limited to areas not etched in the silicon device layer.

1.2 Process Overview

The PiezoMUMPs process is a simple 5-mask level SOI patterning and etching process derived from work performed at MEMSCAP. This process flow is intended to add functionality to the SOIMUMPs process. The process flow described below is designed to introduce users to this micromachining process. The text is supplemented by drawings that show the process flow in the context of building a resonating cantilever.

AluminumNitride AlN is a polar compound useful for Piezoelectric MEMS. It has been effective in the development of many useful sensors and actuators. It has a piezoelectric strain coefficient, d_{33} , on the order of 3.4-6.5 (pC/N).

The process begins with 150mm n-type double-side polished Silicon On Insulator wafers, as specified in section 1.1 of this document. The top surface of the Silicon layer is doped by depositing a phosphosilicate glass (PSG) layer and annealing at 1050°C for 1 hour in Argon (Figure 1.2). This PSG layer is then removed via wet chemical etching.

A 2000 Angstrom thermal oxide is grown, patterned and the drawn area, defined by the PADOXIDE mask, is remains after etching a reactive ion etch (RIE).

The first deposited layer in the process is the piezoelectric layer, PZFILM, (Figure 1.4). It is 0.5 microns of Aluminum Nitride, AlN. It is patterned, wet etched, and followed by a solvent resist strip.

The second deposited layer in the process is the Pad Metal (Figure 1.5). A metal stack of 20 nm of chrome and 1 μm of aluminum is patterned through a liftoff process. 3 μm lines with 3 μm space features may be patterned with a 3 μm alignment tolerance to the Device layer. This metal area must be covered during the subsequent Deep Reactive Ion Etch (Deep RIE). Hence, it is limited to relatively large areas in the actuator. Because this metal is exposed to high temperature during the subsequent process, surface roughness tends to be higher and not suitable for low-loss optical mirror applications.

Silicon is lithographically patterned with the fourth mask level, SOI, and etched using Deep RIE (Figure 1.6). This etch is performed using Inductively Coupled Plasma (ICP) technology; a special SOI recipe is used to virtually eliminate any undercutting of the Silicon layer when the etch reaches the Buried Oxide.

Next, a front side protection material is applied to the top surface of the Silicon layer. The wafers are then reversed, and the Substrate layer is lithographically patterned from the bottom side using the fifth mask level, TRENCH (Figure 1.8). This pattern is then etched into the Bottom Side Oxide layer using Reactive Ion Etching (RIE). A DRIE silicon etch is subsequently used to etch these features completely through the Substrate layer. A wet oxide etch process is then used to remove the Buried Oxide layer in the regions defined by the TRENCH mask (Figure 1.9). The front side protection material is then stripped in a dry etch process. This “releases” any mechanical structures in the Silicon layer that are located over through-holes defined in the Substrate layer.

The wafers are then diced using a laser, sorted and shipped to the PiezoMUMPs user.

The following provides a graphical representation of the process steps.

Silicon Doping

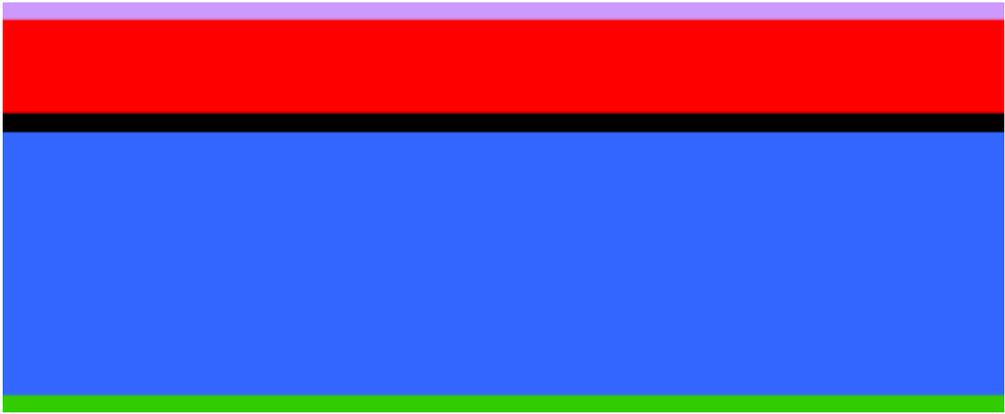


FIGURE 1.2. A phosphosilicate glass layer (PSG) is deposited, and the wafers are annealed at 1050°C for 1 hour in Argon to drive the Phosphorous dopant into the top surface of the Silicon layer. The PSG layer is subsequently removed using wet chemical etching. Note: A Bottom Side Oxide layer is initially present on the starting substrates.

Thermal Oxide	Mask Level: PADOXIDE
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FIGURE 1.3. A 2000 Angstrom thermal oxide is grown. The wafers are then coated with positive photoresist and lithographically patterned by exposing the photoresist with light through the first level mask (PADOXIDE), and then developing it. The oxide is wet-etched. That is followed by an acid resist strip.

Piezoelectric Film Liftoff	Mask Level: PZFILM
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FIGURE 1.4. The film consisting of piezoelectric aluminum nitride is deposited over the wafers by reactive sputtering. The wafers are then coated with positive photoresist and lithographically patterned by exposing the photoresist with light through the second level mask (PZFILM), and then developing it. The material is wet-etched. That is followed by a solvent resist strip.

Pad Metal Liftoff	Mask Level: PADMETAL
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FIGURE 1.5. The wafers are coated with negative photoresist and lithographically patterned by exposing the photoresist with light through the third level mask (PADMETAL), and then developing it. A metal stack consisting of 20 nm chrome and 1000 nm aluminum is deposited over the photoresist pattern by beam evaporation. The photoresist is then dissolved to leave behind metal in the opened areas.

Silicon Patterning	Mask Level: SOI
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FIGURE 1.6. The wafers are coated with UV-sensitive photoresist and lithographically patterned by exposing the photoresist to UV light through the fourth level mask (SOI), and then developing it. The photoresist in exposed areas is removed, leaving behind a patterned photoresist mask for etching. The oxide layer is RIE etched. Deep reactive ion etching (DRIE) is used to etch the Silicon down to the Oxide layer. After etching, the photoresist is chemically stripped.

Polyimide Coat	
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FIGURE 1.7. A front side protection material is applied to the top surface of the patterned Silicon layer. This is a polyimide coat that will hold the wafer together through subsequent trench etching.

Substrate Patterning	Mask Level: TRENCH
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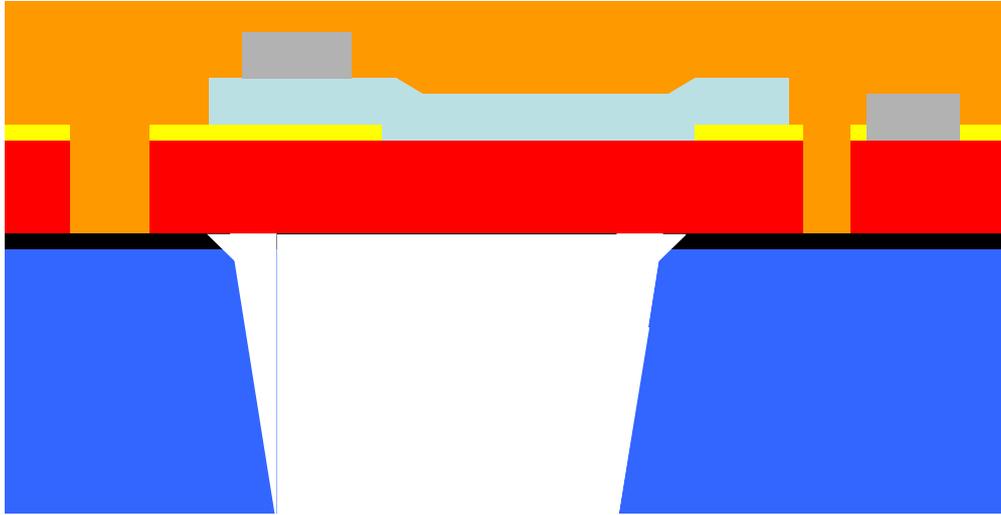


FIGURE 1.8. The bottom side of the wafers are coated with photoresist and the fifth level (TRENCH) is lithographically patterned. Reactive ion etching (RIE) is used to remove the Bottom Side Oxide layer. A DRIE silicon etch is subsequently used to etch completely through the Substrate layer, stopping on the Oxide layer. After the etch is completed, the photoresist is removed. A wet oxide etch process is then used to remove the Oxide layer in the regions defined by the TRENCH mask.

“Release” – Protection layer and Oxide layer removal

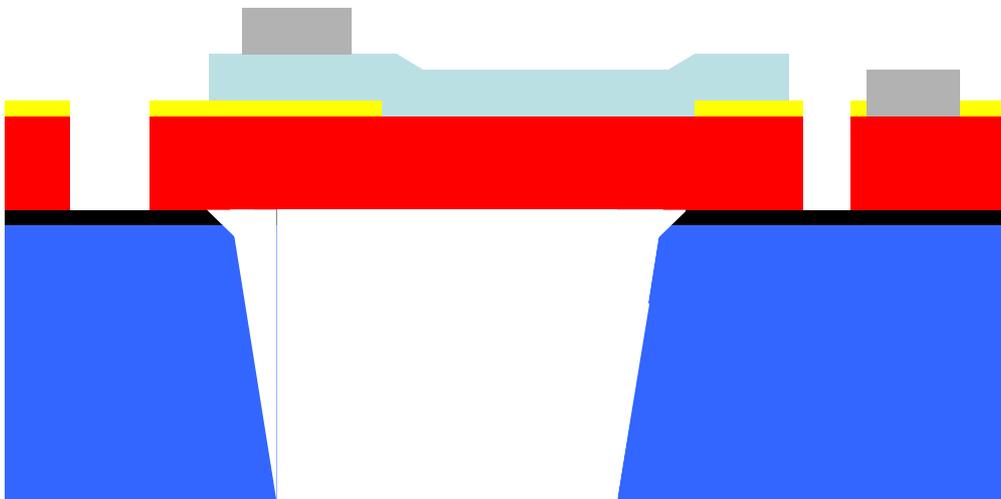


FIGURE 1.9. The front side protection material is then stripped using a dry etch process.

	Silicon		Substrate		Bottom Oxide		Pad Metal
	Oxide		PiezoMaterial		Pad Oxide		Frontside Protection Material

Chapter 2

PiezoMUMPs Design Rules and Considerations

2.1 Introduction

The purpose of the design rules is to ensure the greatest possibility of successful fabrication. The rules have evolved through process development and the experience of the MEMSCAP staff. The design rules are a set of requirements that are defined by the limits of the process (i.e. the stable process window) that in turn are defined by the capabilities of the individual process steps. In general, minimum design rules are defined by the resolution and alignment capabilities of the lithography and resolution and uniformity of the etching systems. This section of the document describes the design rules that exist for the PiezoMUMPs micromachining process.

Design rules in the document define the minimum feature sizes and spaces for all levels and overlay accuracies between relevant levels. The **minimum line widths and spaces are mandatory rules**. Mandatory rules are given to ensure that all layouts will remain compatible with MEMSCAP MEMS' lithographic and etch process tolerances. Violation of minimum line/space rules will result in missing, undersized, oversized or fused features. **Please note: The minimum geometry allowed should not be confused with the nominal geometry a designer uses. Minimum geometries should only be used where absolutely necessary. MEMSCAP has successfully fabricated to these minimums in certain designs and features however, due to the variety of designs on a MUMPs mask set, the etch tolerances will vary from design to design, and die to die. When size is not an issue, the feature should be designed larger than the minimum allowed value. Successful fabrication is entirely design-dependent; as such, customers should be aware that not all designs will fabricate successfully at the minimum line widths. Users of this process should conservatively plan for more than one design-fabrication cycle to ensure successful fabrication of a particular device.**

Finally, there are a few things to keep in mind regarding naming conventions. Lithography levels (i.e. names for each masking level) will be written in upper case. When referring to a specific layer of material the material will be typed in lower case with the first letter capitalized. For example SOI refers to the masking level for patterning the Silicon layer (Silicon). Table 2.1 outlines the material layer names, thicknesses and the lithography levels associated with those layers.

Material Layer	Thickness (μm)	Lithography Level Name	Lithography Level Purpose	Comments
Pad oxide	.2	PADOXIDE	Electrically isolate piezoelectric and PadMetal layers from Silicon	
Piezoelectric Metal	.5	PZFILM	Provide metal for piezoelectric devices	
Pad Metal	1.02	PADMETAL	Provide metal for electrical interconnects	20 nm Cr 1000 nm Al
Silicon	10.0	SOI	Define structures in Silicon layer of SOI wafer	
Oxide	1.0			
Substrate	400	TRENCH	Define through-hole structures in Substrate layer of SOI wafer	

TABLE 2.1. Layer names, thicknesses and lithography levels

2.2 Design Rules

Table 2.2 lists the cross-reference between the MEMSCAP descriptive name, the CIF name and the GDS level number. These are the level names and numbers referred to in the process guide and in any communications you may have with MEMSCAP MEMS' layout support. Please adopt this naming scheme on your own layout system to minimize confusion when you transfer your data file to MEMSCAP for fabrication. The table also lists the associated design rules for that level. These are mandatory rules. Explanations for these rules are discussed in the following sections.

Mnemonic level name	CIF level name	GDS level number	Min. feature (μm)	Min. space (μm)	Max. feature length (μm)	Max. patterned (etched) area
PADOXIDE	POX	10	5	5	Unlimited	N/A
PZFILM	PZF	20	10	10	5000	N/A
PADMETAL	PAD	30	3	3	5000	N/A
SOI	SOI	40	2*	2*	Unlimited for width >6μm (See section 2.2.2)	33 mm ² etched area
SOIHOLE	HOLE	41	3	3	N/A	N/A
TRENCH	TRCH	50	200	200	5000	35 mm ² etched area

TABLE 2.2. MEMSCAP level name, CIF and GDSII™ level designation, and associated design rules. See following sections for explanation of design rules.

It should be noted that the photo masking process used by MEMSCAP is capable of rendering arcs and non-rectangular polygons. You are welcome and encouraged to include non-Manhattan geometries as part of your submission. Keep in mind, however, that the masks are printed with a 0.25 μm spot size and all features are limited by this registration. To minimize vertex snapping errors in the fracturing of the data, please use a 0.25 micron grid in layout and avoid rotating cells.

*Due to pixelation of the 0.25 μm resolution photomasks, features and spaces that are drawn on non-orthogonal axes may not print on the wafer at the nominal sizes. In the case of closely spaced SOI features, this can lead to bridging between the features or abnormally small spaces. To minimize the possibility of bridging, it is recommended that for non-orthogonal features, designers default to a 3μm nominal line/space rule for the SOI level rather than the 2μm minimum values

2.2.1 SOI Hole Layer

The SOI hole level (SOIHOLE) is shown as a separate level in order to make layout of SOI easier. The principal purpose of this level is to provide a simple way to extract holes from a digitized feature. The drawing of the hole in a large digitized level can be difficult with some layout systems. MEMSCAP has chosen to define a unique level for drawing holes to simplify this process.

2.2.2 Maximum Feature Length – SOI Level

Table 2.2 indicates that there is no maximum length for features patterned using the SOI layer, as long as those features have a width that is greater than 6 μ m. Silicon features patterned using the SOI layer that are less than 6 μ m may be “released” from the Substrate due to the undercutting of the Oxide layer during the HF vapor removal of the exposed Oxide regions. *(See section 2.6.2 “Silicon Layer Release and Anchor”).*

“Long” released Silicon structures have a tendency to curl out of plane due to the intrinsic stresses in the Silicon layer, and the surface stress caused by the doping process. The amount of out-of-plane distortion will depend on the length and design of the released structures. For example, 2 μ m Silicon beams that are anchored at one end will curl out-of-plane to a greater degree than 2 μ m Silicon beams that are anchored at both ends. To minimize these effects, an initial conservative guideline for SOI patterns that are less than 6 μ m in width, is to use a maximum length of 100 μ m if the structure is anchored at one end only and 500 μ m if the structure is anchored at two (or more) ends. MEMSCAP will continue to analyze this effect, and will update these guidelines as additional data is collected.

2.2.3 Maximum Feature Length – TRENCH level

The maximum feature length rule in Table 2.2 for the TRENCH is intended to ensure the sturdiness of the SOI wafer following the DRIE etching processes. Features longer than the maximum value could compromise the mechanical integrity of the substrates, leading to chip or wafer breakage.

2.2.4 Maximum Patterned Area

The uniformity of the DRIE etching processes is strongly dependent upon feature size and the amount of silicon area that is etched. In order to minimize non-uniformities and ensure that the pattern from one chip design does not influence the etch results of a neighboring chip design, we require that the total area of silicon that is etched (as defined by the relevant mask pattern) be constrained as follows:

SOI Mask Layer:	<i>Area of Silicon etched < 33mm² (33% of Chip Area)</i>
TRENCH Mask Layer:	<i>Area of Substrate etched < 35mm² (35% of Chip Area)</i>

TABLE 2.3. Mandatory rules related to total area of the SOI and TRENCH layers.

2.3 Rule Nomenclature

This document uses nomenclature that may not be familiar to some users. The nomenclature is based on Boolean operators that are used in a design rule checker. There are two basic operators used to describe the rules: enclose and spacing. The following diagrams explain the nomenclature and describe the operators and rule.

Enclose L2 by L1 (Figure 2.3.1). The operator defines a boundary by which layer L1 must surround layer L2. The boundary has an associated minimum value, A.

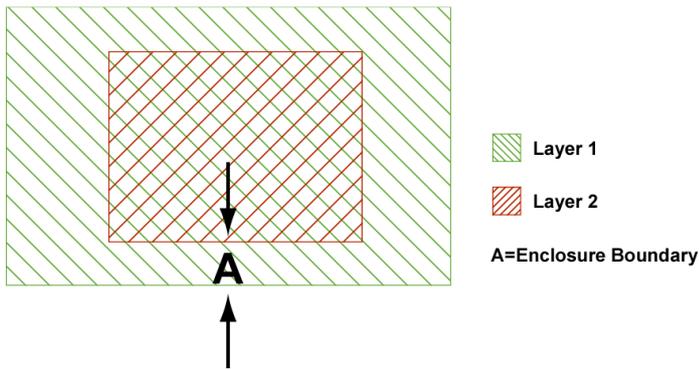


FIGURE 2.3.1. Enclose Layer2 by Layer1. A = minimum boundary dimension.

Spacing L1 to L2 (Figure 2.3.2). The operator defines the spacing between two layers L1 and L2. The spacing has an associated minimum value, B.

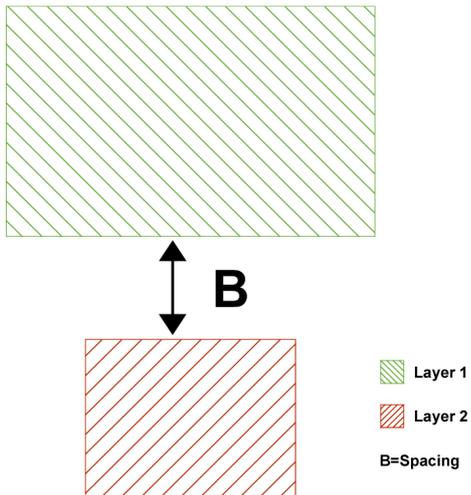


FIGURE 2.3.2. Spacing Layer1 to Layer2. B = minimum spacing

2.4 Level to Level Design Rules

The level to level design rules are listed in Table 2.4. The rules are given in each line of the table along with a figure number and a rule letter. Figures 2.4.1 and 2.4.2 are cross sections and plan views of various “common” design structures that illustrate the rules. The rule letters point out which dimensions on the plan view pertain to the specific rule, and the corresponding verbal explanation of that rule. Please note that the drawings show how the films relate to each other up to that point of processing. For clarity, the drawings do not necessarily represent true or completed structures. Also, of importance, the plan views show the drawn (digitized) layout and cross sections show the resulting structures. This should help you better visualize the rules in layout form. Mandatory rules are in red.

Rule	Rule Letter	Figure #	Min. Value (µm)
SOI enclose PADOX	A	2.4.2	3
PADOX space to PZFILM	B	2.4.2	5
PADOX space to PADMETAL	C	2.4.1	5
PADOX enclose PZFILM	D	2.4.1	5
PADOX enclose PADMETAL	E	2.4.2	4
SOI enclose PZFILM	F	2.4.2	5
PZFILM enclose PADMETAL	G	2.4.1	4
PADMETAL cut into PZFILM	H	2.4.2	5
SOI enclose PadMETAL	I	2.4.2	3

TABLE 2.4 Level to Level Design Rules

- A. Rule A ensures the PADOXIDE does not cross into the SOI Etch area.
- B. Rule B is a guideline to ensure the piezoelectric layer does not interact with the PADOXIDE. Again this is an advisory rule not a mandatory rule.
- C. Rule C is a guideline to ensure the Pad Metal layer does not interact with the PADOXIDE. Again this is an advisory rule not a mandatory rule.
- D. Rule D ensures the PZFILM is completely on PADOX and will not make contact to the SOI layer.
- E. Rule E ensures the PADMETAL is completely on PADOX and will not make contact to the SOI layer.
- F. Rule F ensures the piezoelectric layer PZFILM is not exposed to the SOI etch. This is a mandatory rule.
- G. Rule G ensures the PADMETAL is completely upon the PZFILM. This is an advisory rule.
- H. Rule H ensures contact is made between the PADMETAL and the PZFILM. This is for routing purposes. This is an advisory rule.
- I. Rule I ensures the Pad Metal is not exposed to the SOI etch. This is a mandatory rule.

NOTE: The design rules governing the trench layer (TRENCH) will be described separately in section 2.5.2.

PadMetal Electrical Contact

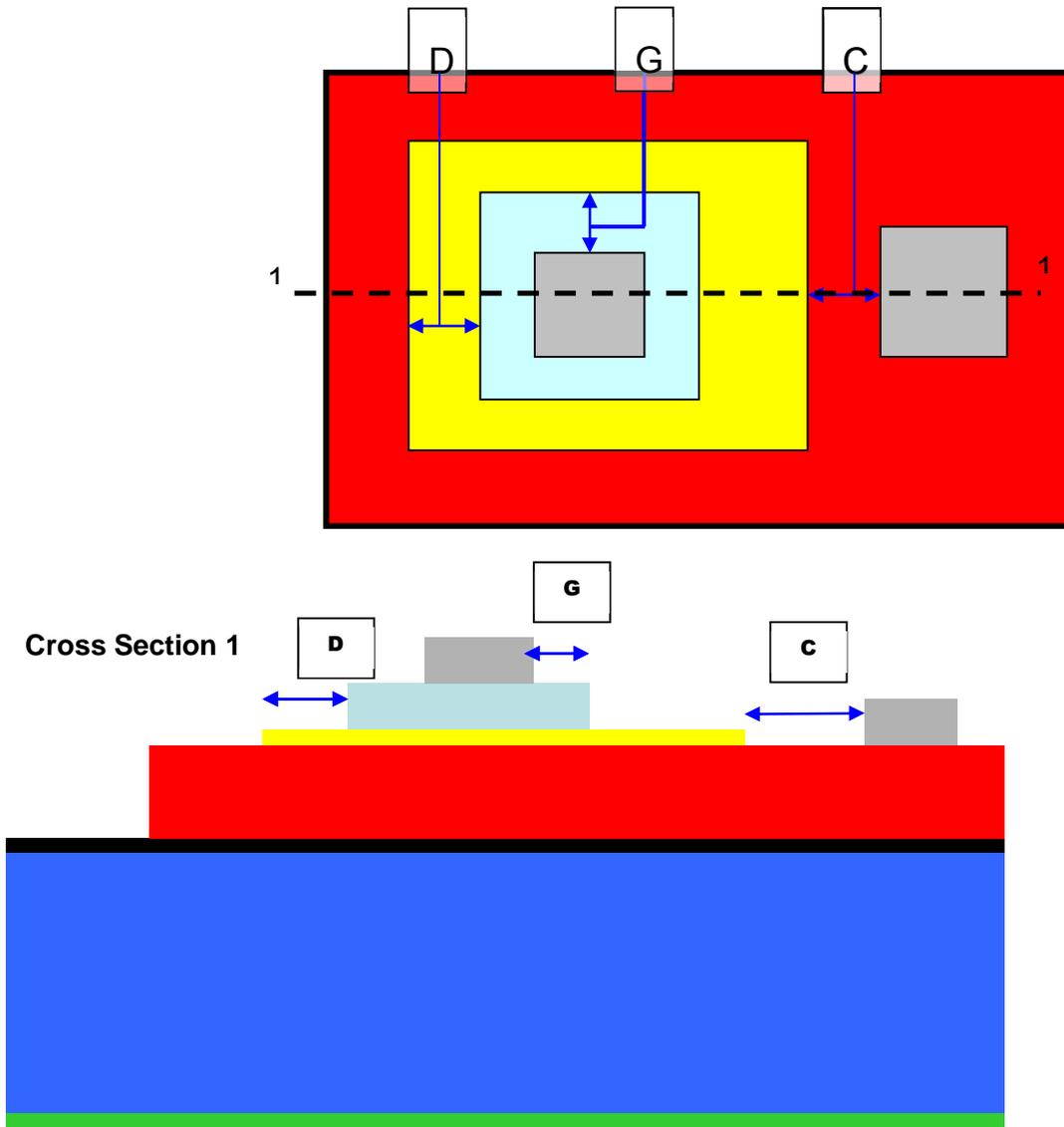


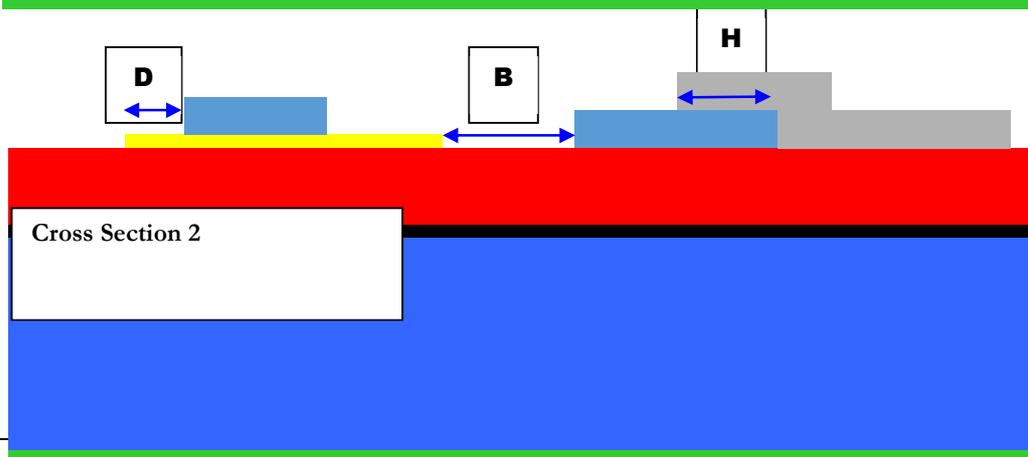
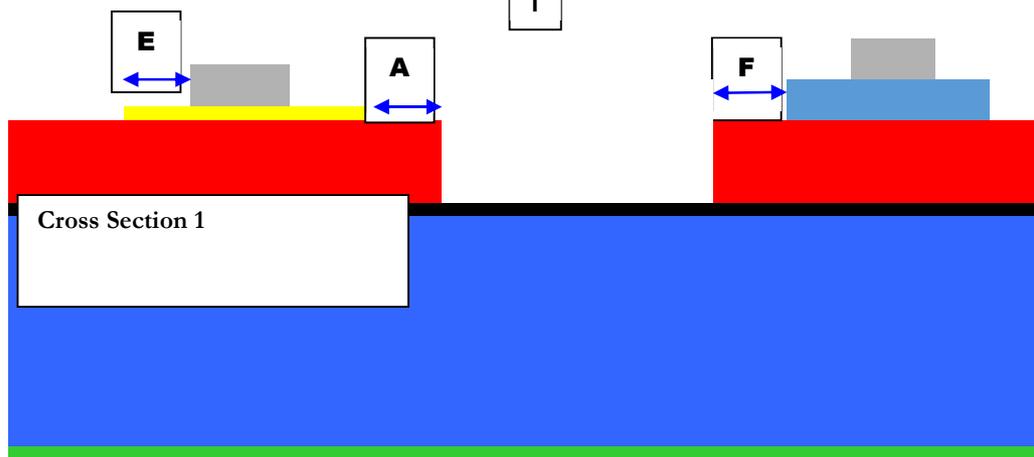
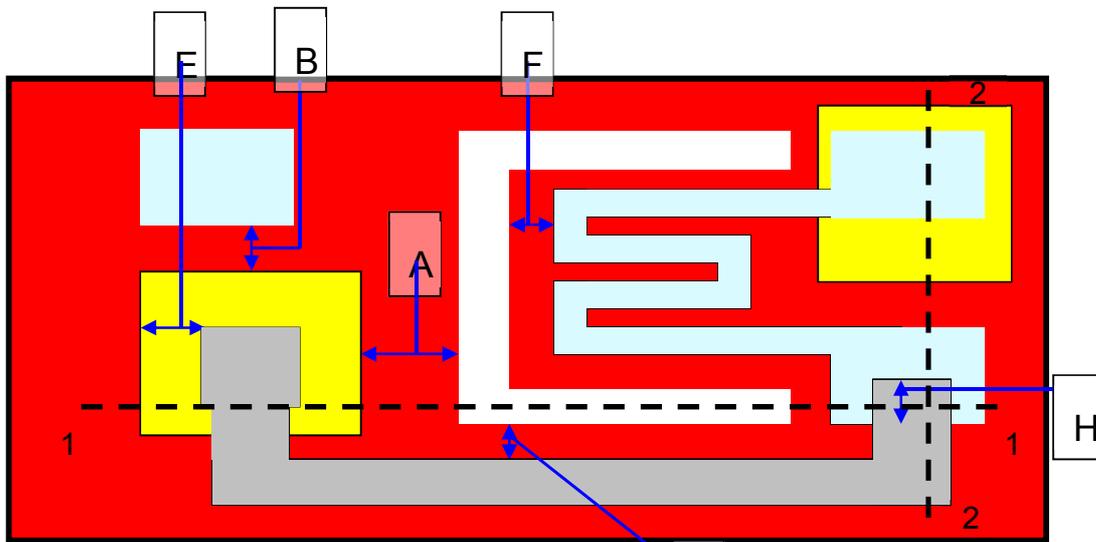
FIGURE 2.4.1.

C: PADOX space to PADMETAL $> 5.0\mu\text{m}$. The amount of space between the PADMETAL and PADOX to ensure the Pad Metal layer does not interact with the PADOXIDE.

D: PADOX enclose PZFILM $> 5.0\mu\text{m}$. The amount that PADOX must extend beyond the edge of PZFILM to ensure the piezoelectric layer is not in electrical contact with SOL.

G: PZFILM enclose PADMETAL $> 4.0\mu\text{m}$. The amount that PZFILM must extend beyond the edge of PADMETAL to ensure complete coverage of the PADMETAL.

	Silicon		Substrate		Bottom Oxide		Pad Metal
	Oxide		PiezoMaterial		Pad Oxide		Frontside Protection Material



	Silicon		Substrate		Bottom Oxide		Pad Metal
	Oxide		PiezoMaterial		Pad Oxide		Frontside Protection Material

FIGURE 2.4.2.

- A: **SOI enclose PADOX** > 3.0 μm . The amount of space between the SOI Etched area and PADOX to ensure the PADOXIDE does not cross into the SOI Etch area
- B: **PADOX space to PZFILM** > 5.0 μm . The amount of space between PADOX and the piezoelectric layer to ensure the piezoelectric layer does not interact with the PADOXIDE.
- E: **PADOX enclose PADMETAL** > 4.0 μm . The amount that PADOX must extend beyond the edge of PADMETAL to ensure the pad metal is completely on the PADOX.
- F: **SOI enclose PZFILM** > 5.0 μm . The amount of space between the SOI Etched area and PZFILM to ensure the PZFILM does not cross into the SOI Etch area.
- H: **PADMETAL cut into PZFILM** > 5.0 μm . The amount of overlap of the PZFILM and the PADMETAL to ensure an electrical contact between the two layers.
- I: **SOI enclose PADMETAL** > 3.0 μm . The amount of space between the SOI Etched area and PADMETAL to ensure the PADMETAL does not cross into the SOI Etch area.
-

2.5 Level to Level Overlay Rules

In the PiezoMUMPs process, the TRENCH mask level is intended for producing coarse features where tight alignment tolerances are not required. In the fabrication process, the TRENCH level is aligned to the SOI mask level. Table 2.5 summarizes the overlay tolerances between these mask levels, and the following sections explain these values.

Layer Combination	Center to Center Overlay Tolerance (μm)	Edge to Edge Bias (μm)
PZFILM to SOI	± 5	± 5
PADMETAL to SOI	± 3	± 3
TRENCH to SOI	± 5	< 50

TABLE 2.5. Level to Level Overlay Rules

2.5.1 PADMETAL and PZFILM to SOI Overlay

Figure 2.5.1 illustrates the PADMETAL to SOI overlay tolerances described in Table 2.5. The “Edge-to-Edge” overlay tolerance accounts for the lithography alignment between the PADMETAL and SOI. **PADMETAL must not extend over the SOI edge during DRIE to avoid masking. This is a mandatory rule. To reiterate, PADMETAL must be enclosed by SOI on all edges by at least 3 microns.**

The PZFILM is treated in a similar matter as the PADMETAL with regard to the SOI edge. **It, the PZFILM, must be enclosed by SOI on all edges by at least 5 microns.**

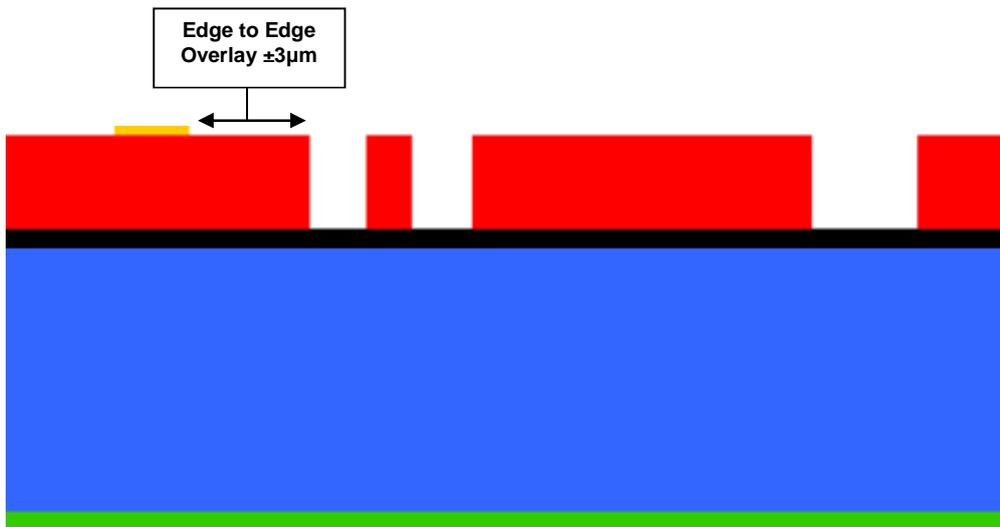


FIGURE 2.5.1. Illustration of the PADMETAL to SOI overlay tolerances given in Table 2.5

2.5.2 TRENCH to SOI Overlay

Figure 2.5.2 illustrates the TRENCH to SOI overlay tolerances described in Table 2.5. The “Center to Center” overlay tolerance accounts for the bottom side to top side lithography alignment between the TRENCH and SOI mask levels. The TRENCH to SOI “Edge to Edge” bias accounts for the etch profile of the through holes in the Substrate layer and the “blow-out” of the etch profile at the Substrate – Oxide interface.

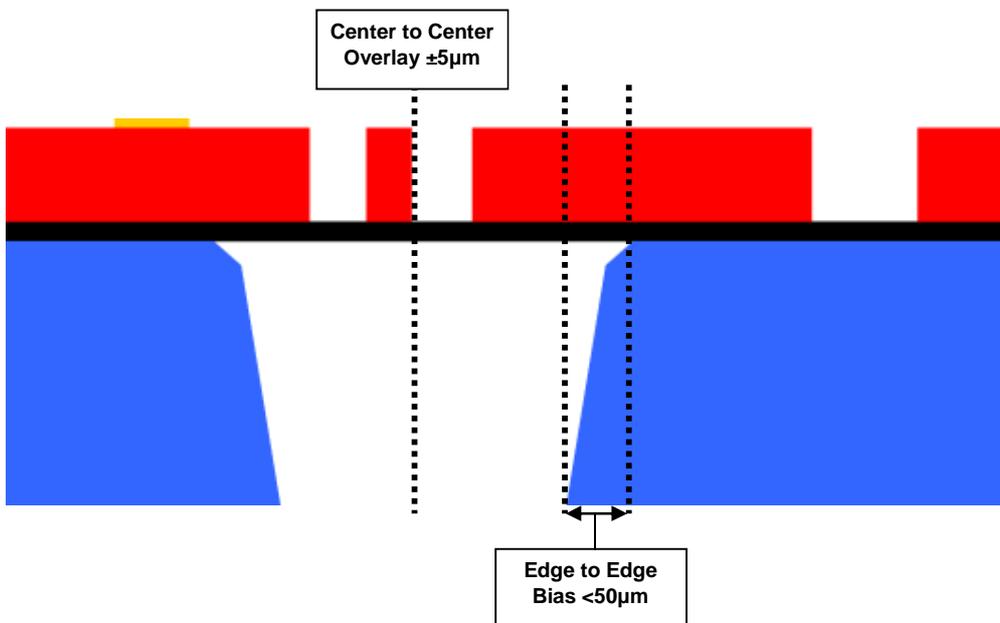


FIGURE 2.5.2. Illustration of the TRENCH to SOI overlay tolerances given in Table 2.5.

2.6 Beyond the Design Rules

Section 2.6 is highly recommended reading for any PiezoMUMPs user, novice or experienced. It includes information that will optimize your PiezoMUMPs design for success, and should prevent several common design errors.

2.6.1 Layout convention

For the PADOXIDE, PZFILM, and PADMETAL, and SOI levels, the mask is light field. For this level, draw (i.e. digitize) the feature you want to keep. The TRENCH level is dark field. For the TRENCH, draw the trench you want to etch. It is imperative that these conventions be followed for your devices to be fabricated correctly.

2.6.2 Silicon Layer Release and Anchor

The “release” of structures in the Silicon layer is accomplished by placing the structures to be released over a TRENCH feature in the substrate. A significant deviation from the SOIMUMPs process occurs at this point. The buried oxide will be etched with the front side protective layer still in place so only features with trench layer beneath them will be released.

To ensure anchoring of Silicon features to the substrate, the SOI feature size should be placed greater than 50 μm from the edge of a TRENCH feature.

2.6.3 Electrical Isolation and Routing

Unless PadOxide is used as an insulating material, there is no insulating layer between the Metal and the Silicon, two adjacent PZFILM or PAD METAL features on the top surface of the Silicon layer will be electrically connected due to the surface doping of the Silicon. As such, patterns in the SOI mask level should be used for electrical isolation between adjacent structures.

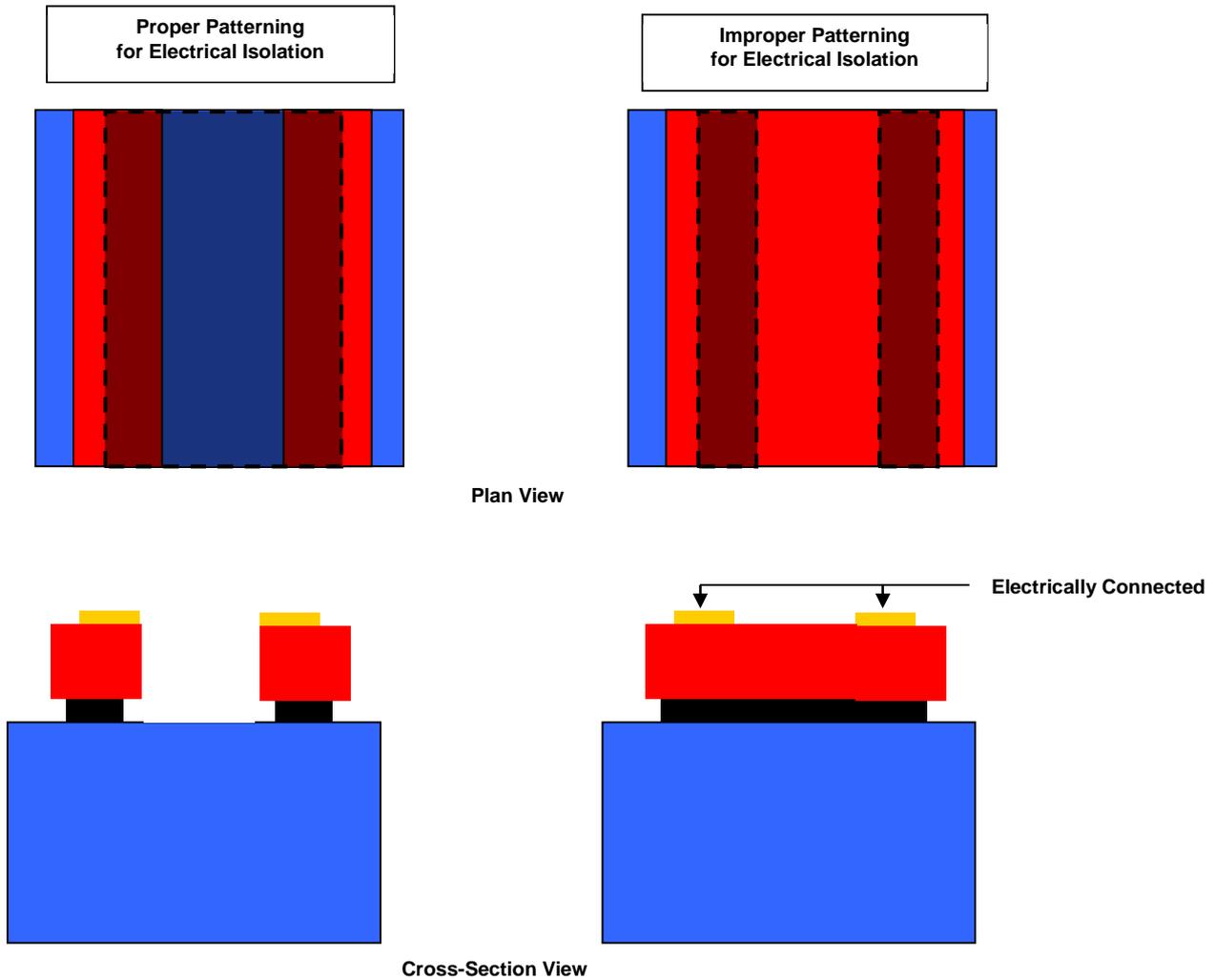


FIGURE 2.6.3. Proper and Improper patterning for electrical isolation

Figure 2.6.3 illustrates proper and improper patterning of the SOI, Piezo-electric Film or PAD METAL levels for electrical isolation. It is acceptable to overlay patterns in the PAD METAL mask levels with routing patterns in the SOI mask level to lower the overall resistance of electrical routing paths

2.6.4 Design Features to Avoid Lateral Stiction of Released Silicon Structures

Closely-spaced, long, narrow beams in the Silicon layer may have a tendency to stick together in the release process. For these types of structures, this lateral stiction can often be avoided by incorporating “dimple-like” features into the design. Dimple protrusions reduce the amount of surface area that can come into contact during the release process. (For experienced MUMPs® users, this is analogous to the dimple structures that are used in the polysilicon surface micromachining process to avoid stiction of polysilicon structures to the substrate). Figure 2.6.4 illustrates an example of incorporating dimple features in the SOI mask level to reduce lateral stiction effects in adjacent beams.



FIGURE 2.6.4. Example of dimple features in the SOI Mask level to reduce lateral stiction affects during release.

2.6.5 TRENCH Pattern Constraints and Full Thickness Suspended Structures

For those familiar with SOIMUMPs, this new process allows for one substantial deviation from the normal SIOMUMPs allowable trenches. Full thickness suspended structures are allowed in PiezoMUMPs. The guidelines for these features will initially be quite conservative until some experimental data can be examined to determine what can and cannot be done. Because of the nature of these substrate masses and their respective support structures, it is difficult to predict the survivability of any particular pattern. The addition of multiple masses to a larger fully isolated trench structure will also markedly decrease the yield. As such, MEMSCAP will make no claims on the reliability of such structures. Figure 2.6.5A illustrates an allowable pattern in the TRENCH level.

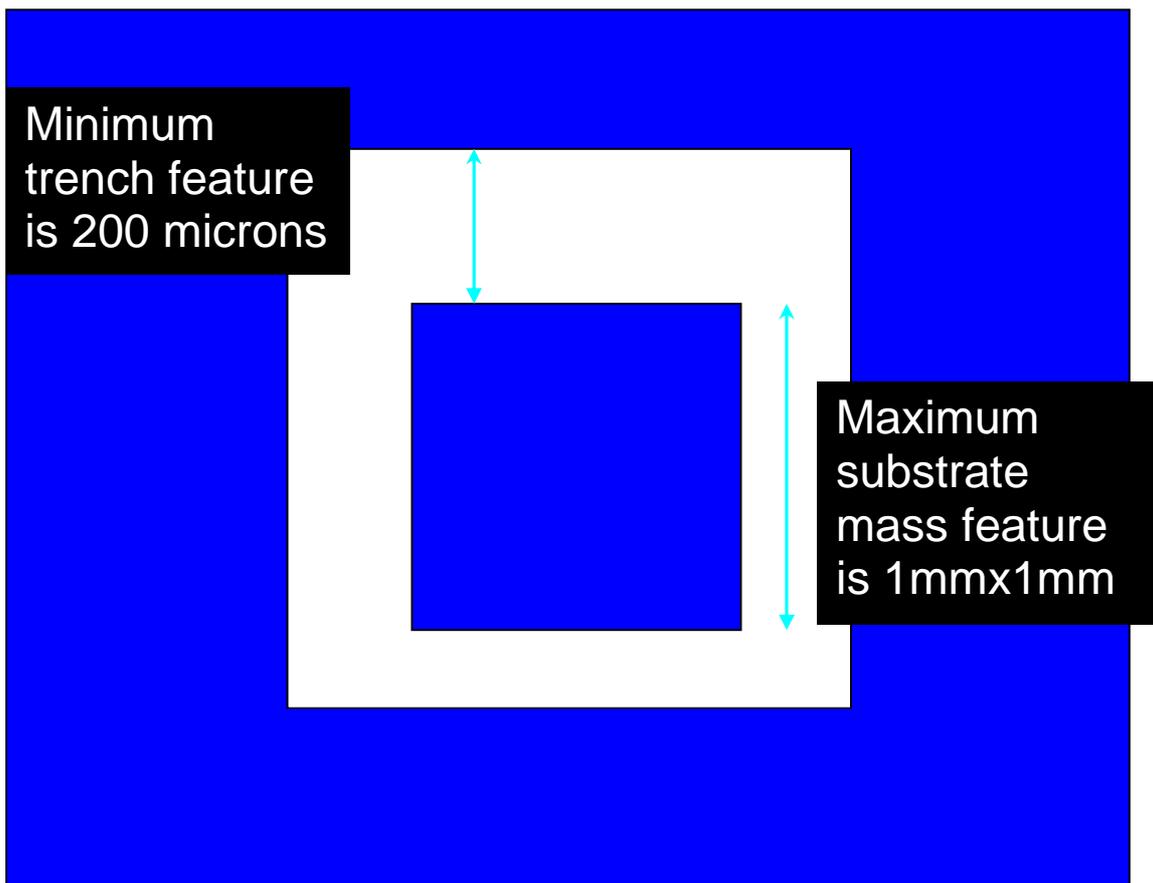


FIGURE 2.6.5A Example of allowable pattern in TRENCH Level which results in a “donut” feature.

A polyimide coat layer is used as a front side protection layer during the trench processing. This layer serves a second purpose as a structure layer. The donut features in the trench often coincide with similar features in the SOI and they define the “Full Thickness Suspended Structures.” These structures will severely weaken the substrate and the polyimide will necessarily hold the wafer together. Figure 2.6.5B illustrates a top down and cross-sectional view of an allowable full thickness suspended structure. At features where the SOI etch coincides with the donuts in the trench, the features should be substantially larger. Initially, that minimum etch in SOI should be greater than 200 microns, the minimum trench feature.

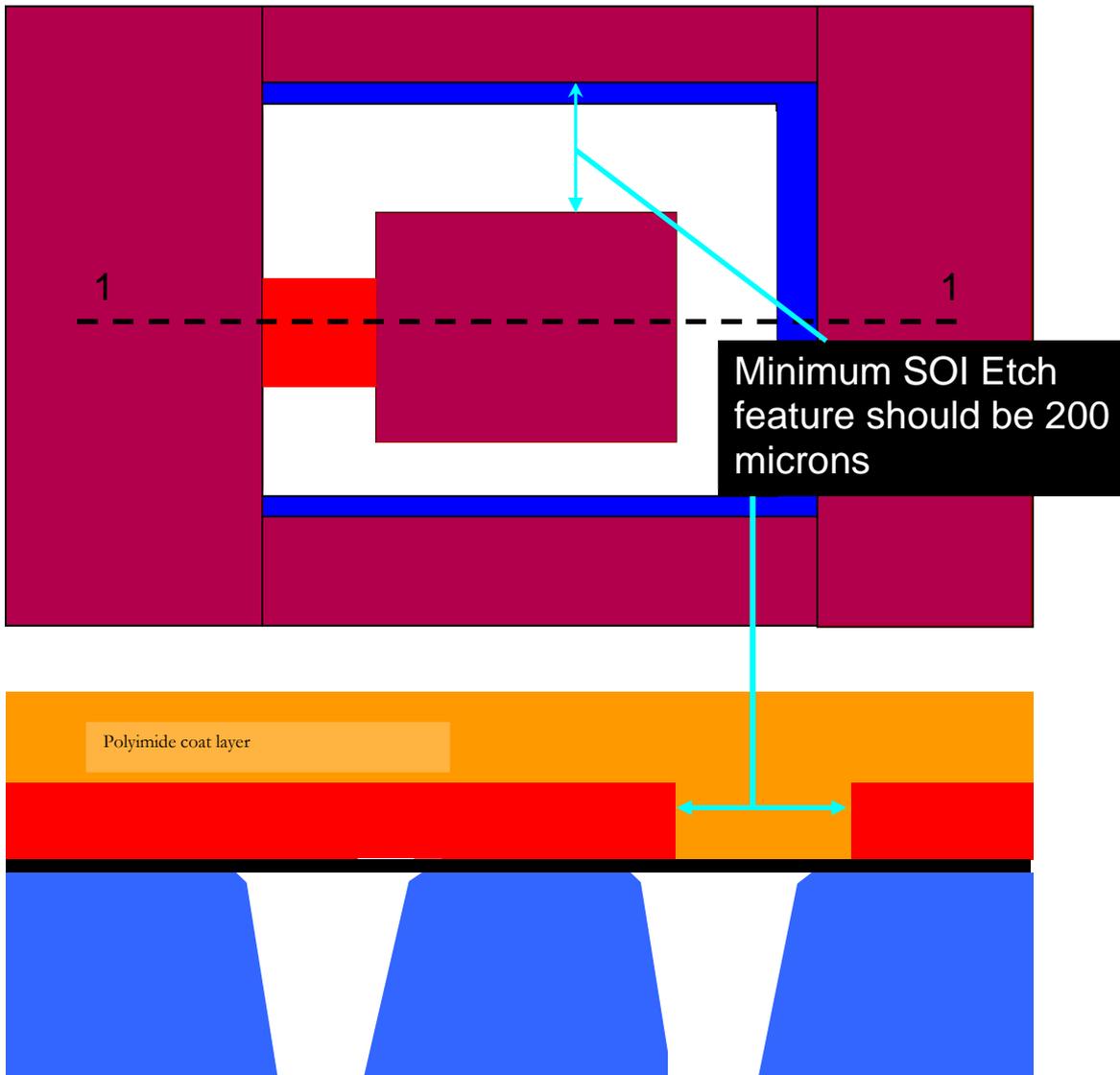


FIGURE 2.6.5B. Example of allowable “full thickness suspended structure”

2.6.6 Anchoring Fragile Released Structures

Suspended structures that are connected to an anchor at 90 degrees can be susceptible to cracking, based on results observed from the early SOIMUMPs runs. Cracking occurs at the corners during application of the protective front side material prior to TRENCH etching. Addition of a fillet at the corners of these devices will mechanically strengthen the point at which cracking originates while having minimal impact on design performance. Figure 2.6.6 shows three possible connections to the anchor for thin beams over a trench. Cracking has occurred in the bottom two beams. For the middle two beams the connection is filleted. The top two beams show a connection that is an improvement if filleting is difficult. The following is a sample layout for this method.

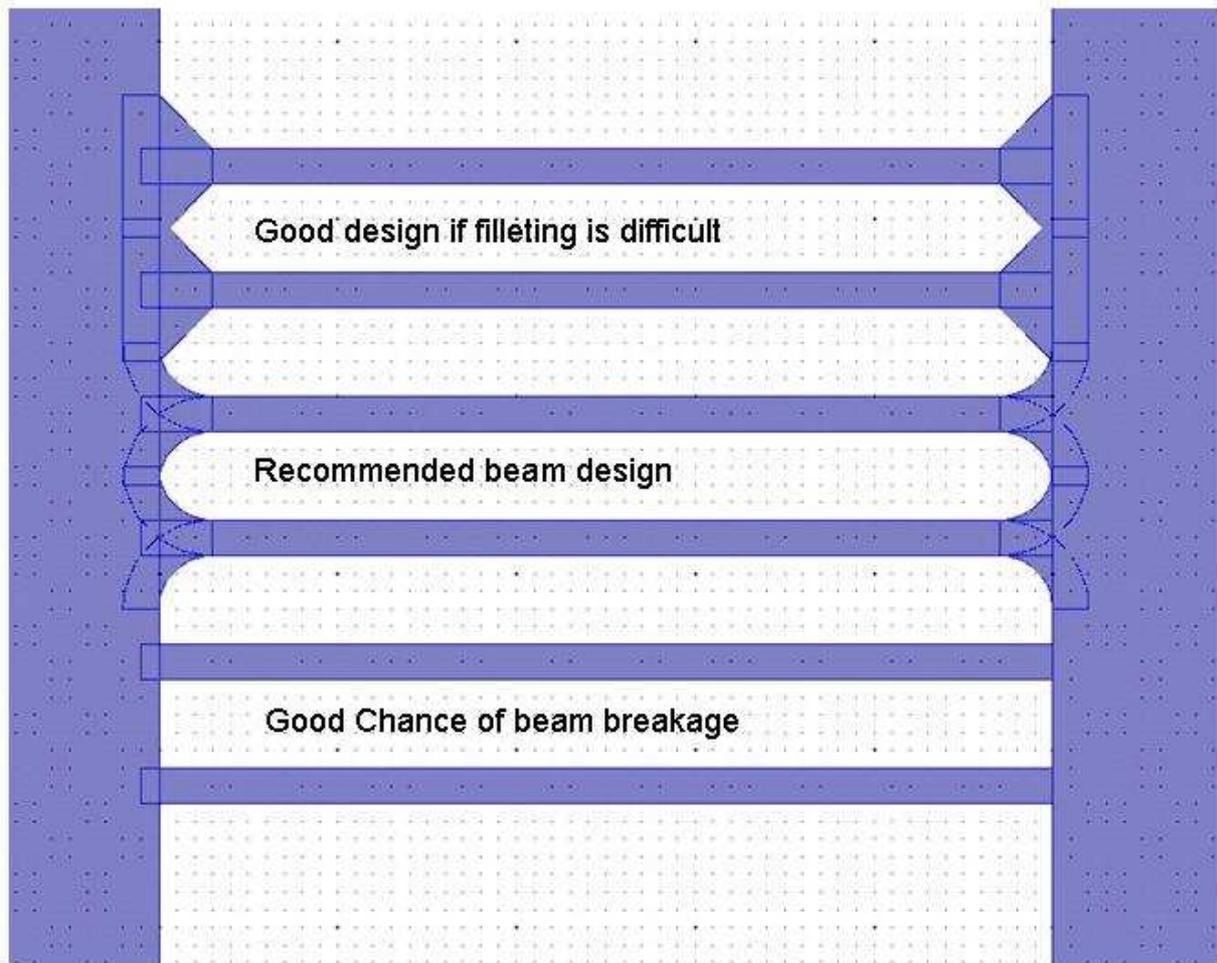


FIGURE 2.6.6. The graphic above depicts recommended design methods for suspended beams. MEMSCAP has observed cracking on structures with square, or 90 degree, edges/anchors.

2.7 Chip Subdicing Options

2.7.1 Laser Subdicing

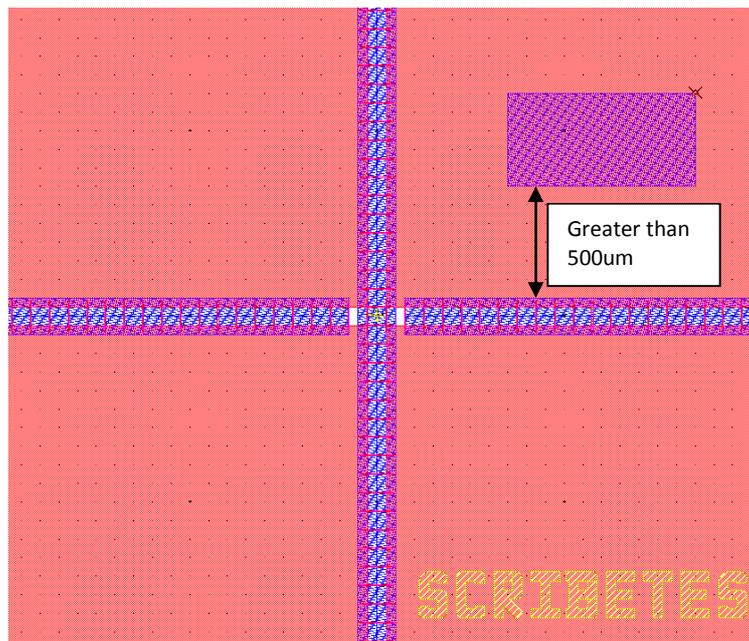
Laser subdicing is available for a fee. This subdicing service allows one or two cuts as specified by the user. If the user opts for a single cut in the middle of the die, two 5.5x11 centimeter subdie would be yielded. Two cuts through the middle of the die, would yield four 5.5x5.5 die.

The dicing streets should be specified by etching a 90 micron or wider street in the SOI layer extended to the edge of the active design area. The TRENCH etch should **not** be used in or near the streets. Furthermore, there should be no metal within 100 microns of the streets.

Please refer to the MUMPs web pages for pricing of this service.

2.7.2 Designed-In Subdicing

By removing silicon in the TRENCH layer and the SOI layer in the same region, the process provides an alternative way of subdividing the die into 2 – 4 pieces. There should be no more than one subdicing trench in either direction. The following is a sample layout for this method.



PiezoMUMPs Sample intersection used to sub-dice a chip. Trench dimension is 200 micron width running the entire length of the chip; however, it should not intersect. The SOI in each quadrant is tied together with 10 micron strips that are laid out at a 100 micron pitch. Other trench features should not be placed within 500 microns from the streets.

As illustrated below in Figure 2.9.1, the actual die size is approximately 11 mm x 11 mm; while the available user area is 9 mm x 9 mm. This leaves about a 1 mm frame of full thickness SOI around the edge of the die. This frame will limit the subdicing of the die but there are two ways to facilitate subdicing. The first is to completely surround the area to be diced with a trench. The second is similar to the illustration shown in this section except the designer

must extend the trench out to 9,65 mm instead of 9 mm. This is the only exception where the user may draw features beyond the 9mm x 9mm space.

Please be advised that this is not a guaranteed process. If subdicing is critical to your final device, we recommend the approach in section 2.7.1.

Using this approach, the die will not be shipped completely separated, as regular users of the other MUMPs processes receive with the saw-diced subdicing method. The customer will need to push the die with his/her thumb or finger from the backside of the dicing tape to separate the subdie, then use tweezers to pull the die from the tape.

2.8 Film Parameters

The thickness and resistivity of relevant layers in the PiezoMUMPs process are summarized in Table 2.7. This data is based on measurements from previous runs.

Film	Thickness (μm)			Sheet Resistance (ohm/sq) or Resistivity (ohm-cm)		
	Min.	Typ.	Max.	Min.	Max.	Comments
Thermal Oxide (.2um)	.195	.205	.21	N/A		Oxide (.2um)
Piezoelectric Film						
Pad Metal	0.47	0.52	0.57	0.045	0.065	ohm/sq
Silicon(10um)	9	10	11	15	25	ohm/sq (N-type at surface post doping)
				1	10	ohm-cm (N-type in bulk)
Oxide (10um)	0.95	1.00	1.05	N/A		
Substrate	395	400	405	1	10	ohm-cm (N-type)

TABLE 2.7. Mechanical and electrical parameters of SOIMUMPs process layers.

2.9 Layout Requirements

2.9.1 Usable Area

The design area for PiezoMUMPs is 9mm x 9mm. Due to the incorporation of an exclusion zone required for the Metal shadow mask bonding process, the actual size of the chips that are shipped to the user is 1.115cm x 1.115cm. (The 9mm x 9mm user design area is centered in the chip). Users are advised to place any critical elements of their designs at least .25 mm away from the edge of the 9mm x 9mm usable area. (See Figure 2.9.1)

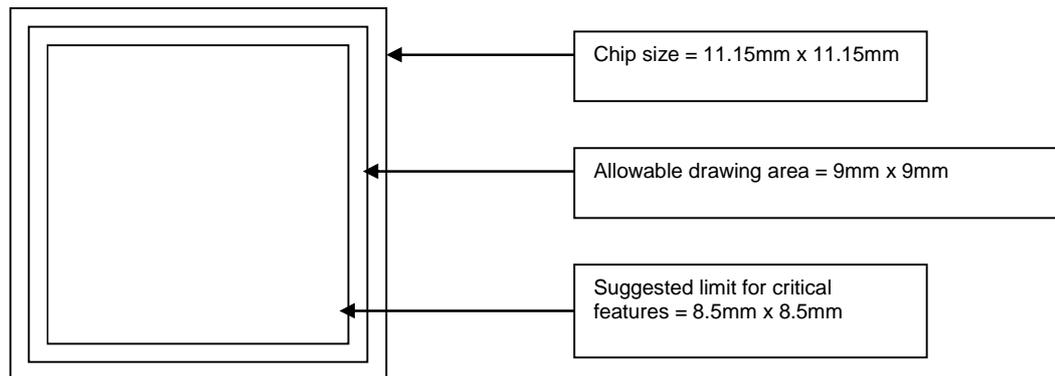


FIGURE 2.9.1: Usable chip area

2.9.2 Cell Name Restrictions

Some errors have occurred in the past due to nonstandard cell names. In order to reduce these errors and the time it takes to translate designs, some guidelines need to be put in place. They are as follows:

1. Cell names should be under 28 characters.
2. Cell names should consist of only the following characters or numerals [a-zA-Z0-9] and the underscore character '_'.

2.9.3 Layer Names

Layouts must use layer names as indicated in Table 2.2. For CIF submissions the indicated names should be used (i.e. for Piezoelectric Film use PZF) and for GDS submissions the correct number must be used. Other layers may be in the design; but they will be ignored. MEMSCAP is not responsible for layers omitted due to failure to comply with naming conventions.

2.9.4 General Layout Tips and Known Software Bugs

Mentor Graphics software is currently used to assemble the PiezoMUMPs wafer layout. It does a reasonable job with most translations; however, there are some additional nuances of which users should be aware.

Keep in mind that these are the bugs that MEMSCAP is aware of - we are not responsible for problems resulting from other bugs not listed here.

1. In GDS, three wire types are allowed, extended, butted, and rounded ends. Rounded ended wires will be converted to a truncated ending. It is strongly suggested that only extended wire types be used with CIF files; otherwise, information may be lost and connections broken.

2. L-Edit versions 7 and 8, up until version 8.22, have a bug. The bug comes from the donut command in L-Edit which becomes a filled circle when written out to gds and translated into other programs. If you use a donut, be sure to use the horizontal or vertical cut commands to break the donut into multiple polygons.
3. There is a bug in L-Edit versions before 8.41 when working with rotated and mirrored instances. If an instance is rotated and mirrored, then saved to gds, the rotation angle will be rounded off to the nearest degree (i.e. an instance is rotated 22.2 degrees and then mirrored, after saving to gds and reading back in, the angle will be changed to 22 degrees).
4. Mentor will create an error if an illegal polygon is produced during translation. Figure 2.6.4 illustrates an example of this problem. Most layout tools deal with this polygon correctly. To fix the problem the points can be made common or the polygons resized slightly. The user will be responsible for making the changes to fix these errors. These types of errors very often occur in lettering and in pictures that have been translated to gds.

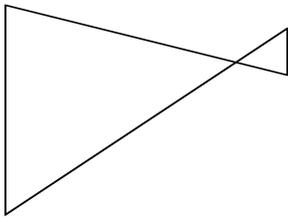


FIGURE 2.6.4A: An Illegal polygon in Mentor.

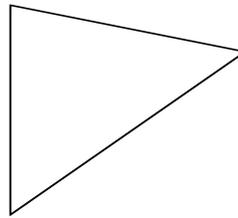


FIGURE 2.6.4B: A Correct polygon.

5. Mentor also has problems with the translations of polygons with numbers of vertices over 1000. These often come from mechanical drawings and should be broken down into smaller polygons before submission.

2.9.5 Design Rule Checking

PLEASE NOTE THAT NO ERROR CHECKING WILL BE DONE ON YOUR DESIGN OTHER THAN THOSE THAT ARE MANDATORY RULES. We have DRC/technology files available for Tanner, Cadence, and Mentor CAD software. To get these, visit the PiezoMUMPs web pages at <http://www.memscap.com> or send an email to info@memscap.com.

2.10 Layout Submission

Before submitting your design, you must reserve your die location at www.memscap.com. Once the reservation is received, MEMSCAP will send a confirmation email with further instructions on how to upload your design.